IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:	10/563,509
Applicants:	Tomohiro URYU et al.
Filing Date:	January 5, 2006
Title:	IMAGE SIGNAL PROCESSING DEVICE
T.C./A.U.:	2629
Examiner:	Randal L. Willis
Confirmation No.:	8639
Notice of Appeal Filed:	November 19, 2010
Docket No.:	MAT-8791US

APPEAL BRIEF UNDER 37 C.F.R. § 41.37

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

S I R :

Appellants hereby request consideration and reversal of the Final Rejection dated August 23, 2010, of claims 1-6.

This Brief is presented in the format required by 37 C.F.R. § 41.37, in order to facilitate review by the Board. In compliance with 37 C.F.R. § 41.37(a)(1), this Brief is being filed within the time allowed for response to the action from which the Appeal was taken or within two months from the date of the Notice of Appeal, whichever is later.

The fees for filing a Brief in support of an Appeal under 37 C.F.R. § 41.20(b)(2), together with any extension fee required in connection with the filing of this Brief, are provided herewith.

I. REAL PARTY IN INTEREST

The real party in interest in this matter is Panasonic corporation by virtue of an assignment recorded on July 14, 2006, at Reel/Frame 017933/0656 and an assignment recorded on October 1, 2008 at Reel/Frame 021897/0689.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences related to the subject matter of this Appeal.

III. STATUS OF CLAIMS

Claims 1-6 are pending in this application and stand rejected. Claims 1-6 are appealed.

IV. STATUS OF AMENDMENTS

The present application is under final rejection. All amendments have been entered.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The invention (as shown in Fig. 4) provides an image signal processing device that outputs a video signal to a plasma display. The image signal processing device includes a semiconductor circuit 21 having a video signal processing unit 24, 25 and 26 and a control unit 22. The image signal processing device also includes an external memory 23 that is external to the semiconductor circuit 21.

Referring to Fig. 4, control unit 22 controls video signal processing unit 24, 25 and 26 to output a video signal to a plasma display driving circuit 12 (see Fig. 5B where video is output in period A of each field). Control unit 22 receives its control data for controlling 24, 25 and 26 from external memory 22. Specifically, the control data is transferred from external memory 23 to control unit 22 during the vertical blanking period (see Fig. 5B where control data is transferred in period B of each field).

The control data transmitted during vertical blanking period B includes data that needs to be updated in every field (e.g. data d1), and data that does not need to be updated in every field (e.g. data d2). Since data d2 does not need to be updated in every field, it may be divided into a plurality of reduced size data (i.e. smaller pieces) having a common size that corresponds to the length of the vertical blanking period. The divided data may then be transferred in successive fields.

For example, as shown in Figs. 6A, 6B, 6C and 6D, data d2 may be divided into two reduced pieces of data d2-a and d2-b (i.e. d2 is divided in half), and transferred during two successive vertical blanking periods (e.g. data d2-a is transferred during a vertical blanking period in Fig. 6C, and data d2-b is transferred during the following vertical blanking period in Fig. 6D).

In Figs. 6A-6D, data d2 is two times the size of the available portion of the vertical blanking period, and therefore was divided into two pieces having a common size. It is also noted, however, that data d2 may be divided into more than two pieces. For example, if data d2 is four times the size of the available portion of the vertical blanking period, it may be divided into four pieces having a common size (see Fig. 7A-7E where d2 is divided into d2-a, d2-b, d2-c and d2-d). Thus, the data is divided into common size pieces dependent on the length of the vertical blanking time period. See pages 7-11 of Applicants' specification for further support.

Now turning to the independent claims, claim 1 recites: An image signal processing device (Fig. 4) comprising: a semiconductor integrated circuit (21, Fig. 4) having: a video signal processing unit (24, 25 and 26, Fig. 4) for outputting video output data to a display device (12, Fig. 4) in a plurality of fields (Fig. 5b); and a control unit (22, Fig. 4) for holding data for controlling an operation of the video signal processing unit (24, 25 and 26, Fig. 4); and an external memory (23, Fig. 4) that is disposed outside the semiconductor integrated circuit (21, Fig. 4), holds control data to be fed to the control unit (22, Fig. 4), and allows data read to be controlled by the control unit (22, Fig. 4), wherein data transferred between the external memory (23, Fig. 4) and the control unit (22, Fig. 4) has data that must be updated in every field (data d1-A, d1-B in Figs. 6A-6D) of the plurality of fields and data that does not need to be updated in every field (data d2 in Figs. 6A-6D) of the plurality of fields, and is transferred in a vertical blanking time period (period B in Fig. 5B) of the video output data, and the data that does not need to be updated in every field is divided into a plurality of reduced size data (data d2-a and d2-b in Fig. 6c and 6D) having a common size corresponding to a length of the vertical blanking time period, the plurality of reduced size data assigned to the plurality of fields respectively, and transferred.

Independent claim 4 recites: An image signal processing device (Fig. 4) for a display device performing a display according to a subfield driving method comprising: a semiconductor integrated circuit (21, Fig. 4) having: a video signal processing unit (24, 25 and 26, Fig. 4) for outputting video output data to the display device (12, Fig. 4) in a plurality of fields; and a control unit (22, Fig. 4) for holding data for controlling an operation of the video signal processing unit (24, 25 and 26, Fig. 4); and an external memory (23, Fig. 4) that is disposed outside the semiconductor integrated circuit (21, Fig. 4), holds control data to be fed to the control unit (22, Fig. 4), and allows data read to be controlled by the control unit (22, Fig. 4), wherein the video signal processing unit includes: an image quality correcting circuit (24, Fig. 4) for signal processing to correct image quality of video signal data input into the video signal processing unit, a subfield converting circuit (25, Fig. 4) for generating a signal for every subfield of the plurality of fields based on output data from the image quality correcting circuit (24, Fig. 4), a first memory (24a, Fig. 4) for holding data, that must be updated in every field of the plurality of fields, required by the image quality correcting circuit (24, Fig. 4), and a second memory (25a, Fig. 4) for holding data, that does not need to be updated in every field of the plurality of fields, required by the subfield converting circuit (25, Fig. 4), wherein the semiconductor integrated circuit (21, Fig. 4) has a plurality of terminals and at least two of the plurality of terminals (27b, 27c, Fig. 4) are used for both outputting the video output data output from the video signal processing unit and transferring data between the external memory (23, Fig. 4) and the control unit (22, Fig. 4), and the data transferred between the external memory (23, Fig. 4) and the control unit (23, Fig. 4) has the data that must be updated in every field (data d1-A, d1-B in Figs. 6A-6D) and the data that does not need to be updated in every field (data d2 in Figs. 6A-6D), and is transferred in a vertical blanking time period (period B in Fig. 5B) of the video output data, and ROM data stored in the external memory in the vertical blanking time period are acquired into the second memory (25a, Fig. 4) for holding the data required by the subfield converting circuit (25, Fig. 4) in every field and an operation of the subfield converting circuit (25, Fig. 4) is controlled based on the ROM data, the data that does not need to be updated in every field is divided into a plurality of data (data d2-a and d2-b in Fig. 6c and 6D) having a common size corresponding to a length of the vertical blanking time period, assigned to the plurality of fields respectively, and transferred.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-6 are rejected under 35 U.S.C. 103(a) as obvious over Miura (W003044766 in which U.S. 2004/0263496 is used as an English translation) in view of Fumoto (U.S. 5,200,738) and "What is Asynchronous Transfer Mode" by Ken Black.

VII. ARGUMENT

Neither Miura, Fumoto, Ken Black or their combination disclose or suggest,

> ... the data that does not need to be updated in every field is divided into a plurality of reduced size data having a common size corresponding to a length of the vertical blanking time period, the plurality of reduced size data assigned to the plurality of fields respectively, and transferred.

as required by claim 1. Claim 4 while not identical has similar features.

The issue here is that Appellants claim an image processing device that divides data into a plurality of reduced size data having a common size. In contrast, Miura's static control data has to be divided into a plurality of reduced size data having different sizes based on the type of data (not based on a common size), otherwise the transmissions will be incomplete.

Appellants believe the Examiner has incorrectly combined the prior art references because Miura's static control data has to be divided based on the type of data (not based on a common size of the vertical blanking), otherwise the complexity of the transmitter and receiver will be increased. If Miura's static control data is broken into common size data, then how would it be reconstructed at the receiver? For example, if the video control data, light source control data and display mode control data are broken up based on a common size, then partial pieces of the data

will be transmitted during different frames. The partial pieces must then be reconstructed at the receiver. In the Examiner's "reconstruction" of the prior art, the Examiner has provided no explanation of how the partial pieces would be reconstructed. Appellants maintain that without such an explanation, the "reconstruction" would be inoperative and thus the operability of the patents being combined would be destroyed.

Miura's system which teaches static control data broken up into reduced size data is combined with Fumoto and Ken Black's systems which suggests transmitting common size data over a vertical blanking period between frames. Specifically, in the Final Office Action, the Examiner states that it would be obvious to modify Miura's system to divide the static control data into common sizes and transmit them over the vertical blanking period.

Miura's system, as shown in Fig. 4B, includes static control data. Specifically, the static control data includes different types of data (i.e., video control data 15A, light control source data 15B and display mode control data 15C). As shown in Miura's Fig. 5B, the static control data is broken up (by type) and transmitted in successive frames (i.e., the video control data B0, B1 and B2 are transmitted during the first frame, light source control data B3, B4 and B5 are transmitted during the second frame and display mode control data B6 and B7 are transmitted during the third frame).

As shown in Fig. 3 and described in col. 4, Fumoto suggests transmitting data over a vertical blanking period. Specifically, col. 4 of Fumoto suggests changing the contents of 102B and control registers 105 during a vertical blanking period.

Black suggests an asynchronous transfer mode (ATM) where data is transmitted. Specifically, Black suggests that encoding data in asynchronous transfer mode is consistent because each cell is 53 bytes in length (the cells have a common data length).

Appellants' claim 1 recites an image processing device that transmits data over a vertical blanking period. Specifically, data is divided into a plurality of

reduced size data which have a common size corresponding to the length of the vertical blanking time period.

As shown in Appellants' Figs. 6A-6D, data d2 is broken up into a plurality of reduced size data d2-A and d2-B which have a common size corresponding to the vertical blanking time period. Another example is at least shown in Figs. 7A-7E where the data d2 is broken up into reduced size data d2-A, d2-B, d2-C and d2-D which all have a common size. By dividing the data into reduced size data having a common size (e.g. common number of bytes), the entire vertical blanking time period (which has a common size between each frame) may be utilized more efficiently. See page 10 of Applicants' specification for further support.

On pages 4 and 5 of the Final Office Action, the Examiner states that it would be obvious to modify Miura's system (based on Fumoto and Black) to divide the static control data into data blocks having a common size. One of ordinary skill in the art, however, would not modify Miura's system to divide the static control data into common size data blocks, because Miura's static control data would have to be divided based on the type (i.e. based on whether it is video control, light source, or display mode data).

For example, as shown in Miura's Fig. 4B, video control data, light source control data and display mode control data do not have a common size. Specifically, the video control data ([B0,B1,B2]) and light source control data ([B3,B4,B5]) are three blocks in size, whereas the display mode control data ([B6,B7,]) is only two blocks in size.

It is important in Miura's system to break the static control data based on the type of data so that the data transmissions are complete (i.e., all of the video control data, light source control data or display mode control data is sent in a single frame and are not broken up over multiple frames). This is at least shown in Miura's Fig. 5B where the three different types of data are transmitted in three different frames regardless of their size.

In one example, if the static control data ([B0, B1, B2]) is divided into blocks having a common size (e.g., size 2), then blocks B0 and B1 will be sent in the first frame and blocks B2 and B3 will be sent in the second frame. Thus, the video

control data will only be partially sent in the first frame (i.e., B0 and B1 will be in the first frame, but B2 will not be transmitted until the second frame).

In another example, if the static control data is broken into blocks having size a common size (e.g. size 3), then the video control data and light source control data will be sent as complete data, however, display mode control data will not consume an entire vertical blanking period (i.e., the vertical blanking period will have capacity for three blocks, but the display mode control data only has two blocks B6 and B7, thereby wasting transmission space).

Thus, if the data is divided into too small of a size, then incomplete data will be transmitted and then have to be reconstructed by the receiver, thereby greatly increasing the complexity of the receiver. If the blocks are divided into large data blocks, then some of the transmission space in the vertical blanking period may be wasted thereby greatly reducing the efficiency of the system.

Since Miura teaches a system for dividing static control data based on the type of data, one of ordinary skill in the art would not modify Miura to divide the data based on a common size (modifying Miura to divide data with a common size would increase the complexity while decreasing the efficiency of the receiver). Neither Miura, Fumoto, Black nor their combination suggests the features in Applicants' independent claims. Thus, the claims are patentable over the art of record for at least the reasons set forth above.

Respectfully submitted,

Lawrence E. Ashery, Reg. No. 34,515
Attorney for Applicants

RAE/sh

Dated: March 7, 2011

P.O. Box 980
Valley Forge, PA 19482-0980
(610) 407-0700

VIII. CLAIMS APPENDIX

1. An image signal processing device comprising:

a semiconductor integrated circuit having:

a video signal processing unit for outputting video output data to a display device in a plurality of fields; and

a control unit for holding data for controlling an operation of the video signal processing unit; and

an external memory that is disposed outside the semiconductor integrated circuit, holds control data to be fed to the control unit, and allows data read to be controlled by the control unit,

wherein data transferred between the external memory and the control unit has data that must be updated in every field of the plurality of fields and data that does not need to be updated in every field of the plurality of fields, and is transferred in a vertical blanking time period of the video output data, and

the data that does not need to be updated in every field is divided into a plurality of reduced size data having a common size corresponding to a length of the vertical blanking time period, the plurality of reduced size data assigned to the plurality of fields respectively, and transferred.

2. The image signal processing device according to claim 1,

wherein the video signal processing unit has a memory for holding the data that must be updated in every field and a memory for holding the data that does not need to be updated in every field.

3. The image signal processing device according to claim 1,

wherein the data is divided into the plurality of reduced size data to ensure that each one of the plurality of data can be transferred between the external memory and the control unit, respectively during successive vertical blanking periods.

4. An image signal processing device for a display device performing a display according to a subfield driving method comprising:

a semiconductor integrated circuit having:

a video signal processing unit for outputting video output data to the display device in a plurality of fields; and

a control unit for holding data for controlling an operation of the video signal processing unit; and

an external memory that is disposed outside the semiconductor integrated circuit, holds control data to be fed to the control unit, and allows data read to be controlled by the control unit,

wherein the video signal processing unit includes:

an image quality correcting circuit for signal processing to correct image quality of video signal data input into the video signal processing unit,

a subfield converting circuit for generating a signal for every subfield of the plurality of fields based on output data from the image quality correcting circuit,

a first memory for holding data, that must be updated in every field of the plurality of fields, required by the image quality correcting circuit, and

a second memory for holding data, that does not need to be updated in every field of the plurality of fields, required by the subfield converting circuit,

wherein the semiconductor integrated circuit has a plurality of terminals and at least two of the plurality of terminals are used for both outputting the video output data output from the video signal processing unit and transferring data between the external memory and the control unit, and

the data transferred between the external memory and the control unit has the data that must be updated in every field and the data that does not need to be updated in every field, and is transferred in a vertical blanking time period of the video output data, and

ROM data stored in the external memory in the vertical blanking time period are acquired into the second memory for holding the data required by the subfield converting circuit in every field and an operation of the subfield converting circuit is controlled based on the ROM data,

the data that does not need to be updated in every field is divided into a plurality of data having a common size corresponding to a length of the vertical blanking time period, assigned to the plurality of fields respectively, and transferred.

5. The image signal processing device according to claim 4, wherein a line for outputting the video output data is connected with a line for outputting the data output from the external memory.

6. The image signal processing device according to claim 4, wherein the data that does not need to be updated in every field is divided into a plurality of reduced size data corresponding to a length of the vertical blanking time period, the plurality of reduced size data assigned to the plurality of fields respectively, and transferred.

IX. EVIDENCE APPENDIX

None

X. RELATED PROCEEDINGS APPENDIX

None